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APPLICATION
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DOHERTY AMPLIFIER**
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SIGNAL AMPLIFIER USING A DOHERTY AMPLIFIER

Field of the Invention

5 , The present invention relates to a signal amplifier; and, more particularly, to a signal amplifier employing a Doherty amplifier suitable for use in a mobile communications terminal.

10 Background of the Invention

As is well known in the art, a Doherty amplifier is a high efficiency amplifier capable of performing an input and output impedance matching process. The Doherty amplifier
15 generally uses two amplifiers, a carrier amplifier and a peaking amplifier, and controls the load line impedance of the carrier amplifier, depending on the power level of an input signal and the amount of current provided from the peaking amplifier to the load line. To attain such a high
20 efficiency performance over a wide input signal bandwidth, the Doherty amplifier employs a technique where the carrier amplifier and the peaking amplifier are connected in parallel to each other by a quarter-wave transmission line ($\lambda/4$ line).

25 The Doherty amplifier was used in earlier days as an amplitude modulation (AM) transmitter of a broadcasting

apparatus using a high-power low-frequency/middle-frequency (LF/MF) vacuum tube. Then, various suggestions have been made to apply the Doherty amplifier to a solid-state high-power transmitter.

5 In Fig. 1, there is provided a signal amplifier using a conventional Doherty amplifier.

As shown in Fig. 1, the signal amplifier includes a splitter 10, a transmission line 15, a Doherty amplifier 20, a first load line 30 and a second load line 40. The Doherty
10 amplifier 20 has a carrier amplifier 23 and a peaking amplifier 24. Further, the carrier amplifier 23 includes an input matching circuit 21 and a transistor 22; and the peaking amplifier 24 similarly includes an input matching circuit 21' and a transistor 22'.

15 In the conventional Doherty amplifier, an input signal is split into two signals at the splitter 10 and inputted into the Doherty amplifier 20. One of the two signals is fed to the carrier amplifier 23 and the other signal is delayed by the transmission line 15 having characteristic
20 impedance Z_a and then fed to the peaking amplifier 24. The delay of the signal may be adjusted so that the input of the peaking amplifier 24 lags the input of the carrier amplifier 23 by 90 degrees.

The transistors 22 and 22' of the carrier amplifier 23
25 and the peaking amplifier 24 are respectively fed with a predetermined base bias voltage regardless of the power

level of the input signal. The peaking amplifier 24 provides current to the second load line 40 according to the power level of the input signal. As the amount of the current supplied to the second load line 40 varies, the impedance of the first load line 30 placed at an output of the carrier amplifier 23 is adjusted so as to control the efficiency of the Doherty amplifier 20. Two quarter-wave transmission lines having characteristic impedances Z_m and Z_b may be used for the first and second load lines 30 and 40 placed at the outputs of the carrier amplifier 23 and the peaking amplifier 24, respectively.

Then, the signals transmitted respectively from the first load line 30 and the peaking amplifier 24 are combined at a combination circuit common node 50 and outputted through the second load line 40.

However, because the aforementioned Doherty amplifier should use an additional quarter-wave transmission line to transform an output impedance to match with 50Ω , wherein 50Ω is a traditional setting for an output impedance, its substantial circuit size tends to be large. For this reason, there is a limitation in using the conventional Doherty amplifier in a mobile communications terminal where the size of a circuit including the amplifier is critical.

And also, because a constant bias voltage is fed to both the carrier amplifier and the peaking amplifier regardless of the power level of the input signal, the

conventional Doherty amplifier is not suitable for application in mobile communications terminals where an input signal frequency varies in a wide range.

5 Summary of the Invention

It is, therefore, a primary object of the present invention to provide a signal amplifier for achieving high linearity and high efficiency by providing a Doherty
10 amplifier with a bias signal varying in accordance with a power level of an input signal and for achieving minimization of the signal amplifier by controlling a characteristic impedance of a Doherty output network arranged at an output of the Doherty amplifier.

15 In accordance with a preferred embodiment of the present invention, there is provided a signal amplifier using a Doherty amplifier, the signal amplifier including a splitter for splitting an input signal into two signals to be transmitted respectively through a first and a second
20 transmission paths; a first and a second bias control networks for generating bias signals corresponding to a power level of the input signal by alternating its operation modes, wherein the power level of the input signal lower than a predetermined threshold level is associated with a
25 low input power drive mode and the power level of the input signal higher than the predetermined threshold level is

associated with a high input power drive mode; a Doherty amplifier including a carrier amplifier for amplifying the signal transmitted through the first transmission path and a peaking amplifier for amplifying the signal transmitted through the second transmission path; and a Doherty output network for matching and outputting signals amplified at the carrier amplifier and the peaking amplifier.

Brief Description of the Drawings

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The above and other objects and features of the present invention will become apparent from the following description of a preferred embodiment given in conjunction with the accompanying drawings, in which:

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Fig. 1 is a circuit diagram showing a signal amplifier using a conventional Doherty amplifier;

Fig. 2 depicts a circuit diagram showing a signal amplifier using a Doherty amplifier in accordance with a preferred embodiment of the present invention; and

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Fig. 3 provides a graph showing an efficiency of the signal amplifier using the Doherty amplifier in accordance with the preferred embodiment of the present invention.

Detailed Description of the Preferred Embodiments

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The preferred embodiment of the present invention will

now be described in detail with reference to the accompanying drawings.

Fig. 2 illustrates a circuit diagram showing a signal amplifier using a Doherty amplifier in accordance with the preferred embodiment of the present invention. As shown in Fig. 2, the signal amplifier includes a splitter 100, an attenuator 110, a first transmission line 120, a Doherty amplifier 200, a first and a second bias control networks 300 and 310, and a Doherty output network 400. The Doherty amplifier 200 includes a carrier amplifier 210 and a peaking amplifier 220. The carrier amplifier 210 has an input matching circuit 211, a driving transistor 212, an inter-stage matching circuit 213, an output transistor 214, and an output matching network 215. Likewise, the peaking amplifier 220 has an input matching circuit 221, a driving transistor 222, an inter-stage matching circuit 223, an output transistor 224, and an output matching network 225. Although the carrier amplifier 210 and the peaking amplifier 220 constructing the Doherty amplifier 200 are described respectively as a two-stage structure having two transistors in Fig. 2, it will be understood by the one skilled in the art that it can be configured in a single-stage or more-than-two-stage structure.

Meanwhile, the splitter 100 may be implemented by using a Wilkinson divider or other passive elements to split an input signal into two signals to be transmitted

respectively through two transmission paths, i.e., a first transmission path and a second transmission path, wherein the attenuator 110 and the carrier amplifier 210 are located on the first transmission path and the first transmission
5 line 120 and the peaking amplifier 220 are located on the second transmission path.

Further, the attenuator 110 may be implemented by using passive elements such as resistors or active elements such as variable gain amplifiers (VGAs), which are arranged
10 on the first transmission path prior to the carrier amplifier 210. The attenuator 110 attenuates the signal transmitted from the splitter 100 and feeds it to the carrier amplifier 210, thereby compensating a gain difference between the first and the second transmission
15 paths. Although the attenuator 110 is placed at an input end of the carrier amplifier 210 on the first transmission path in this embodiment, alternatively, it can be placed at an input end of the peaking amplifier 220 on the second transmission path.

20 The first transmission line 120 is located between the splitter 100 and the peaking amplifier 220 for compensating a time delay and a phase delay between signals transmitted on the first and the second transmission paths, wherein the first transmission line 120 is an offset transmission line
25 having characteristic impedance R_{ip} and phase θ_{ip} , which may be changed appropriately to compensate the time and phase

differences. Further, the first transmission line 120 may be implemented by using lumped elements.

On the other hand, the first bias control network 300 has a V_{contC} pin for receiving a control voltage varying with the power level of the input signal and a V_{refC} pin for providing the carrier amplifier 210 with a base bias voltage varying with the control voltage received at the V_{contC} pin. Further, the second bias control network 310 has a V_{contP} pin for receiving a control voltage whose level is equal to that of the control voltage fed to the V_{contC} pin and a V_{refP} pin for providing the peaking amplifier 220 with a base bias voltage varying with the voltage fed to the V_{contP} pin. That is, each of the first and the second bias control networks 300 and 310 alternates its operation mode between low and high input power drive modes, in accordance with the control voltage provided to the V_{contC} and V_{contP} pins, generates different base bias voltages in accordance with each operation mode and feeds the base bias voltages to the carrier amplifier 210 and the peaking amplifier 220 through the V_{refC} and V_{refP} pins, respectively.

The control voltages fed to the V_{contC} and V_{contP} pins vary with the power level of the input signal. For example, if the input signal has a power level lower than or equal to a predetermined threshold power level, a high voltage such as 2 - 3 V is fed to the first and the second bias control networks 300 and 310. Conversely, if the input signal has a

power level higher than the predetermined threshold power, a low voltage such as 0 V is fed to the first and the second bias control networks 300 and 310.

When a high voltage is fed to the V_{contC} pin, the
5 operation mode of the first bias network 300 is set to the low power drive mode, and, therefore, the bias voltage provided to the carrier amplifier 210 through the V_{refC} pin decreases. Then, collector idle currents of the transistors 212 and 214 are also reduced. Likewise, when a high voltage
10 is applied to the V_{contP} pin, the operation mode of the second bias network 310 is changed to the low power drive mode. Thereafter, the transistors 222 and 224 are biased by the bias voltage supplied through the V_{refP} pin, and it makes the peaking amplifier 220 turned off.

15 On the other hand, when a low voltage 0 V is applied to the V_{contC} and V_{contP} pins, the first and the second bias control networks 300 and 310 respectively change their operation modes to the high power drive mode and provide both the carrier amplifier 210 and the peaking amplifier 220
20 with the base bias voltages through the V_{refC} and V_{refP} pin, to thereby bias the transistors 212, 214, 222 and 224. In this way, the carrier amplifier 210 and the peaking amplifier 220 function as class AB amplifiers, respectively. That is, when the input signal power level is below a
25 predetermined threshold voltage (in case of the low power drive mode), only the carrier amplifier 210 functions as a

conventional Doherty amplifier, entailing in a high efficiency. Further, when the input signal power level is above the predetermined threshold voltage (in case of the high power drive mode), both the carrier amplifier 210 and the peaking amplifier 220 function as class AB amplifiers, attaining a high efficiency and a high linearity, simultaneously.

As shown in Fig. 2, there are several matching circuits, i.e., the input matching circuits 211 and 221, the inter-stage matching circuits 213 and 223, and the output matching circuits 215 and 225 in the Doherty amplifier 200. The input matching circuits 211 and 221 perform a matching of the input signals of the transistors 212 and 222, respectively, and the inter-stage matching circuits 213 and 223 perform a matching of the output signals of the transistors 212 and 222, respectively. The output matching circuits 215 and 225 perform a matching of the output signals of the transistors 214 and 224, respectively.

The carrier amplifier 210 of the Doherty amplifier 200 amplifies signals attenuated at the attenuator 110 and outputs the amplified signals to the Doherty output network 400. Further, the peaking amplifier 220 amplifies the signals compensated at the first transmission line 120 and also outputs the amplified signals to the Doherty output network 400.

The Doherty output network 400, which includes a

plurality of transmission lines having arbitrary lengths, combines the signals amplified at the carrier amplifier 210 and the peaking amplifier 220. In particular, the Doherty output network 400 includes a second transmission line 410
5 having characteristic impedance R_{oc} and phase θ_c , which is arranged at an output end of the carrier amplifier 210, a third transmission line 420 having characteristic impedance R_{op} and phase θ_p , which is arranged at an output end of the peaking amplifier 220 and a fourth transmission line 430
10 having characteristic impedance R_{oc} and phase 90° , which is coupled between the second transmission line 410 and the third transmission line 420. Herein, in order to perform a Doherty operation, the output of the carrier amplifier 210 should be matched with the characteristic impedance R_{oc} of
15 the second transmission line 410, and the output of the peaking amplifier 220 should be also matched with the characteristic impedance R_{op} of the third transmission line 420. These transmission lines 410, 420 and 430 may be implemented by using lumped elements.

20 In the high power drive mode, the signal amplifier of the present invention having the above-mentioned structure is capable of reducing the optimum load impedances because the carrier amplifier 210 and the peaking amplifier 220 are operated as class AB amplifiers simultaneously. For
25 adjusting the reduced optimum load impedance to 50Ω at the output end of the amplifiers 210 and 220, the characteristic

impedance of the second and third transmission lines 410 and 420 may be adjusted by using the following equations:

$$R_{op} = 50 \cdot (1 + \alpha) \quad \text{Eq. (1)}$$

$$R_{oc} = 50 \cdot \frac{1 + \alpha}{\alpha} \quad \text{Eq. (2)}$$

5 where α is a size ratio of the peaking amplifier 220 to the carrier amplifier 210. Accordingly, the Doherty output network 400 may prevent leakages from the output signal of the signal amplifier and achieves a desired load impedance without using an additional quarter-wave line at the output
10 end of the Doherty output network 400. Further, the phases θ_c and θ_p of the second and third transmission lines 410 and 420 are determined by matching the resistive and reactive values of the load impedance, thereby obtaining a highest output power. A method for determining the phases
15 θ_c and θ_p has suggested by Y. Yang, J. Yi, Y.Y. Woo, and B. Kim, in "Optimum Design for Linearity and Efficiency of a Microwave Doherty Amplifier using a New Load Matching Technique", Microwave Journal, pp. 20-36, December 2001.

Fig. 3 shows a graph of power-added efficiency(PAE,%)
20 versus output power level (dBm) for the signal amplifier in accordance with the present invention. In a low power region, since the carrier amplifier 210 functions as a conventional Doherty amplifier and the peaking amplifier 220 is pinched off when the input signal is below the
25 predetermined threshold voltage, the efficiency diagram of

the signal amplifier in accordance with the present invention shows the same graph as that of the conventional Doherty amplifier. Further, the carrier amplifier 210 and peaking amplifier 220 function as class AB amplifiers when
5 the input signal is over the predetermined threshold voltage, so that the signal amplifier of the present invention has as high efficiency as a class AB amplifier in a high power region. Therefore, the graph showing PAE of the signal amplifier in accordance with the present invention is folded
10 near the predetermined input power level and achieves high efficiency in a low input power level and also high efficiency and linearity in a high input power level at the same time. These characteristics are essential for a signal amplifier in a CDMA communications system for which a wide
15 coverage of low power signal transmission is required. Further, by manipulating the characteristic impedance of the second and third transmission lines 410 and 420, an additional quarter-wave line, which is needed for adjusting the impedance reduction to 50Ω in a conventional Doherty
20 amplifier, can be eliminated and, thereby, a minimization of the signal amplifier circuit can be achieved.

While the invention has been shown and described with respect to the preferred embodiment, it will be understood by those skilled in the art that various changes and
25 modifications may be made without departing from the spirit and scope of the invention as defined in the following

claims.